

*Sub A<sup>6</sup>*  
We claim:

1. An integrated circuit, comprising:

a first supply track to be connected to a first supply potential;

a second supply track to be connected to a second supply potential, the first supply potential and the second supply potential supplying a supply voltage, said first supply track and said second supply track forming a first metallic layer;

at least one second metallic layer having at least one third supply track to be connected to one of the first supply potential and the second supply potential and disposed in each case above said first metallic layer; and

at least one first capacitive element disposed below said first metallic layer;

said at least one third supply track and at least one of said first supply track and said second supply track defining at least one second capacitive element, said at least one first capacitive element and said at least one second capacitive element smoothing over the supply voltage.

*a* 2. The integrated circuit according to claim 1,

3. The integrated circuit according to claim <sup>2</sup>1, including an insulating material disposed between said at least one poly section and said first and second supply tracks, said insulating material having a plurality of plated-through holes formed therein connecting said first supply track of said first metal layer to said at least one poly section.

4. The integrated circuit according to claim 1, wherein said at least one second capacitive element is formed by an interaction of said at least one third supply track and said first supply track.

5. The integrated circuit according to claim 1, wherein said at least one second capacitive element is formed by an interaction of said at least one third supply track and said second supply track.

6. The integrated circuit according to claim <sup>2</sup>1, wherein said first capacitive elements and said second capacitive elements each have a capacitive component and a resistive component connected in series with said capacitive component, said resistive component of said second capacitive elements substantially resulting from conductances of said first metallic layer and said at least one second metallic layer, and said resistive component of said first capacitive

elements substantially resulting from conductances of said at least one poly section and of corresponding ones of said doping regions in said substrate.

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~~10~~. The integrated circuit according to claim <sup>6</sup>~~8~~, wherein said resistive component of said first capacitive elements is at least a factor of 10 greater than said resistive component of said second capacitive elements.

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wherein said at least one first capacitive element is connected in parallel with said at least one second capacitive element.

a 3. The integrated circuit according to claim 2, wherein said at least one first capacitive element is one of a plurality of first capacitive elements disposed below both said first supply track and below said second supply track, and said at least one second capacitive element is one of a plurality of second capacitive elements.

4. The integrated circuit according to claim 3, wherein said second capacitive elements each have a capacitance and said first capacitive elements each have a capacitance at least a factor of 10 greater than said capacitance of said second capacitive elements.

Subt a<sup>7</sup> ✓ 5. The integrated circuit according to claim 3, including:

a substrate having doping regions formed therein; and

a polysilicon layer having at least one poly section disposed above said substrate, said first capacitive elements formed by an interaction of said at least one poly section formed in said polysilicon layer and said doping regions formed in said substrate.